# Hybrid Digital Acquisition System Architecture Integrating ASIC-Based Fine Time Resolution With FPGA-Based Coarse Time Resolution

Zaifa Lin, Mingjia Shangguan, and Fuqing Cao

***Abstract*—Digital acquisition systems (DASs) are crucial in fields, such as high-energy physics, communications, medical imaging, industrial control, radar, and lidar technologies, due to their high precision, rapid response, and ability to handle time-sequenced events. These systems are typically implemented using either field-programmable gate arrays (FPGAs) or application-specific integrated circuits (ASICs). FPGA-based high-precision DASs often utilize the FPGA's carry chain. However, the nonuniform delay inherent in the carry chain can affect measurement accuracy. Conversely, ASIC-based systems generally require transferring time tags generated by ASIC to an FPGA for subsequent processing. Given certain transmission capacities, increasing the number of coarse time bits necessitates reducing the number of fine time bits, thereby decreasing resolution or reducing the number of events transmitted per unit time. This article proposes a novel DAS architecture based on fine time measurement using an ASIC and coarse time measurement using an FPGA. This architecture combines the strengths of both ASICs and FPGAs, enabling high-precision event measurement over a wide range with a high counting rate. In addition, a method for relative time tag operation based on this scheme is proposed. Finally, a prototype is designed and tested using ASIC (TDC-GPX2) and Altera's Cyclone 4 series FPGA (EP4CE75F23I7N). This prototype features three input channels and one reference input channel, achieving a least significant bit (LSB) of 20 ps, a measurement accuracy of 30 ps, a measurement range of 430 s, an integral nonlinearity (INL) of [−3, 1.3] LSB, and a differential nonlinearity (DNL) of [−0.6, 0.7] LSB. Long-term stability tests over 21 h showed a peak-to-peak variation of 76 ps. Temperature stability tests conducted within the range of 25 °C–65 °C indicated a peak-to-peak variation of 13 ps. These results demonstrate that the DAS exhibits excellent long-term and temperature stabilities.**

***Index Terms*—Application-specific integrated circuit (ASIC), coarse–fine combination, digital acquisition system (DAS), field-programmable gate array (FPGA), TDC-GPX2, time of flight (TOF), time-to-digital converter (TDC).**

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## NOMENCLATURE

| Parameter | Meaning |
|---|---|
| $AD_1$ | Adder 1. |
| $T_{cmax}$ | Maximum time required for ASIC to perform TDC conversion (ns). |
| $AD_2$ | Adder 2. |
| $T_{cmin}$ | Minimum time required for ASIC to perform TDC conversion (ns). |
| $AD_3$ | Adder 3. |
| $T_{com}$ | Time required to transfer the TT generated by ASIC to FPGA (ns). |
| AG | AND gate. |
| $T_{CT1}$ | Coarse time 1 (ns). |
| $CCM_1$ | Coarse counter module 1. |
| $T_{CT2}$ | Coarse time 2 (ns). |
| $CCM_2$ | Coarse counter module 2. |
| $T_{CT}$ | Coarse time (ns). |
| $C_{co}$ | Coarse clock. |
| $T_{CTA}$ | Coarse time of $Hit_A$ (ns). |
| $CP_1$ | Comparator 1. |
| $T_{CTB}$ | Coarse time of $Hit_B$ (ns). |
| $CP_2$ | Comparator 2. |
| $T_{cov}$ | Time required for ASIC to perform TDC conversion (ns). |
| $C_{re}$ | Reference clock. |
| $T_{D1}$ | Phase delay from $C_{\infty}$ to $C_{re}$ (ns). |
| CTSM | Coarse time selector module. |
| $T_{D2}$ | Delay time from the $F_{CC}$ rising edge to the reading of the $T_{CT}$ in the register (ns). |
| $F_{CC}$ | Flag signal for ASIC conversion completion. |
| $T_{FT}$ | Fine time (ns). |
| FTRM | Fine time receiver module. |
| $T_P$ | Clock period of the $C_{re}$ (ns). |
| $F_{TTR}$ | Flag of reference time tag valid. |
| $T_{pps}$ | Minimum time interval between two consecutive pulses that can be correctly processed by ASIC (ns). |
| HM | Histogram module. |
| TT | Time tag. |
| OSC | Oscillator. |

| | |
|---|---|
| $TT_D$ | Time tag after delay. |
| RTTCM | Relative time tag calculation module. |
| TTFM | Time tag first-in–first-out (FIFO) module. |
| SAM | Send allocation module. |
| $T_{To}$ | Sum of $T_{com}$ and $T_{cov}$ (ns). |
| SFM | Send FIFO module. |
| $TT_R$ | Reference time tag. |
| $SM_1$ | Selection module 1. |
| $TT_{RD1}$ | Reference time tag after first delay. |
| $SM_2$ | Selection module 2. |
| $TT_{RD2}$ | Reference time tag after second delay. |
| STEM | Serial transmission encoding module. |
| $TT_{RE}$ | Relative time tag. |
| TAM | Time assembler module. |
| $T_{TTD}$ | Time delay between TT and $TT_D$ (ns). |

## I. Introduction

TIME-TO-DIGITAL converter (TDC) is a technique used to identify time-sensitive events and obtain a digital representation of the specific time at which these events occur. TDCs are widely used in fields, such as precise time measurement, medical imaging [1], [2], [3], high-energy physics [4], [5], quantum communication [6], [7], fluorescence lifetime imaging microscopy (FLIM) [8], [9], and lidar [10], [11], [12], [13]. TDCs are primarily implemented using two technologies: field-programmable gate arrays (FPGAs) and application-specific integrated circuits (ASICs) [14], [15]. FPGA-based TDCs offer advantages, such as shorter development cycles, lower costs, and greater portability [14]. These TDCs are primarily implemented using delay chains. In Xilinx's 7 series, a resolution of 10 ps can be achieved [16], [17], while in the UltraScale series, resolutions of 5 ps or higher are possible [18], [19]. However, the nonuniform delay in FPGA delay chains results in nonuniform bin widths. For example, the carry delay distribution of Altera's Cyclone series FPGAs ranges from 20 to 180 ps, which degrades the TDC's measurement precision. In addition, their measurement precision is sensitive to process, voltage, and temperature (PVT) [20]. Although various correction methods, such as bin-by-bin calibration and adjusting the FPGA core voltage using external circuits, can mitigate these effects, and they also increase the complexity of the design [21], [22].

In contrast, ASIC-based TDCs, which often work in conjunction with FPGAs, offer high precision, uniform bin widths, and good temperature stability [23], [24], [25], [26], [27]. The time tags obtained by an ASIC typically consist of both a coarse time and a fine time [28]. The more bits used in the coarse time, the larger the range it can represent. However, in most applications, ASIC needs to transmit the tags to an FPGA for further processing. With limited transmission bandwidth, increasing the number of coarse time bits necessitates a reduction in the number of fine time bits (and thus resolution) or a decrease in the number of events that can be transmitted per unit time. This limitation is evident in dedicated TDC chips like TDC-GPX2 [29]. A TDC architecture combining fine time with an ASIC and coarse time with an FPGA is proposed to address the limitations of implementing TDCs using an FPGA or ASIC. This architecture combines the advantages of ASIC and FPGA to achieve high precision, a long measurement range, and high-counting-rate event measurement.

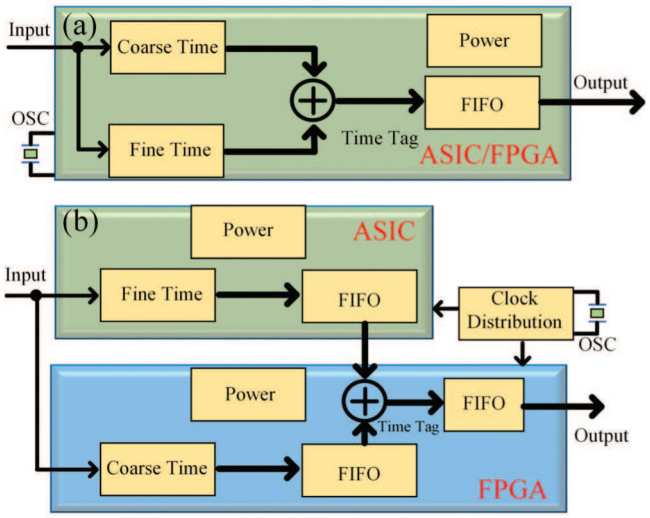


Fig. 1. Comparison between the proposed TDC architecture and the existing architecture. (a) Traditional ASIC-based or FPGA-based TDC architecture. (b) Proposed high-precision DAS employs the coarse–fine time measurement.

In this article, our contributions are as follows.

1) A hybrid TDC implementation framework is proposed and demonstrated (FPGA for coarse counting and ASIC for fine counting).
2) A method for relative time tag computation based on this framework is presented.
3) A prototype of a three-channel acquisition card is developed to evaluate its performance metrics.

## II. Architecture

### A. Principle

The architecture proposed by Nutt [30] achieves high-resolution TDC while accommodating a long measurement range. The traditional implementation of Nutt solutions is mainly based on ASIC or FPGA. As shown in Fig. 1(a), based on the form of ASIC, the acquisition of coarse time and fine time is completed internally in ASIC, and then the coarse time and fine time are merged internally in ASIC as the time tags of the events. This solution has a long development cycle, high development costs, and once ASIC is finalized, it cannot be further modified, resulting in low flexibility. As based on FPGA, the acquisition of coarse time and fine time is implemented internally in FPGA, and then the coarse time and fine time are merged internally in FPGA as the time tags of the events. The development cycle of this solution is relatively short, and the development cost is low, but FPGA has shortcomings compared with ASIC in terms of resolution, nonlinearity, power, temperature, and voltage stability.

As shown in Fig. 1(b), this research innovatively proposes the idea of implementing the Nutt architecture for carrier separation. The fine time part is completed by ASIC, and the coarse time part is completed by FPGA. The fine time completed by ASIC is sent to FPGA through the communication interface, and the coarse time and fine time are merged inside FPGA

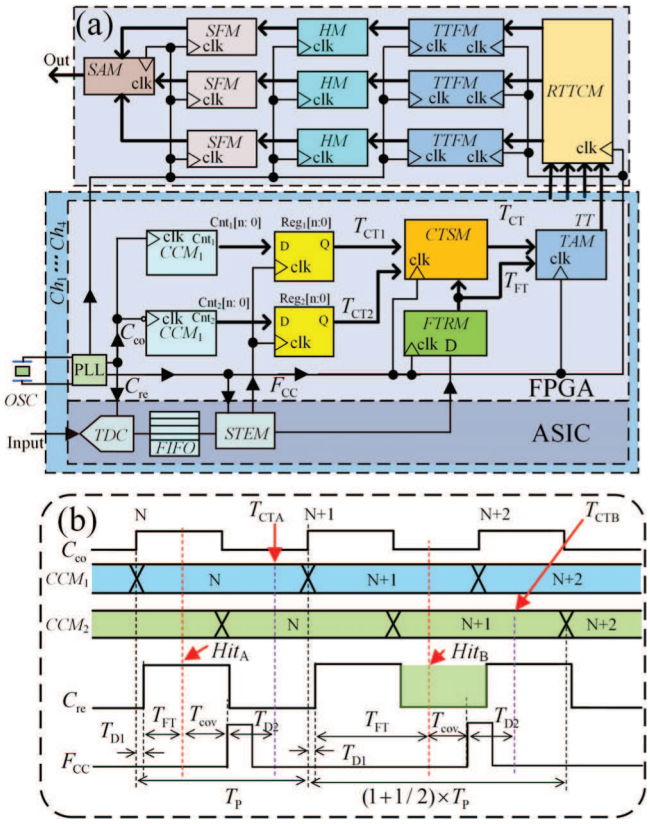


Fig. 2. (a) Schematic of the three-channel acquisition system. (b) Timing diagram of main signals.

as the time tags of the events. The ASIC of this architecture can use commercially available chips, such as TDC-GPX2 or MS1052NA, and FPGA can use various series of FPGAs from mainstream manufacturers, such as Altera and Xilinx. On the basis of the original ASIC, improve the indicator parameters to meet specific TDC requirements. By combing the strengths of ASIC and FPGA, a satisfactory TDC can be achieved in a shorter development cycle.

The abbreviations of the variables mentioned in the following content are detailed in Nomenclature. As illustrated in Fig. 2(a), the event signal is input from the Input interface into ASIC, where it is converted into the fine time tag of the event through the TDC inside ASIC, and the conversion result is stored in the FIFO memory. Then, the data is sent to the FTRM in FPGA through STEM. At the same time, ASIC sends the signal $F_{CC}$ to the registers $Reg_1$ and $Reg_2$ inside FPGA. $Reg_1$ and $Reg_2$ use this signal as the clock signal to read $CCM_1$ and $CCM_2$, and the read results are recorded as $T_{CT1}$ and $T_{CT2}$, respectively, and then transmitted to CTSM. CTSM selects $T_{CT1}$ or $T_{CT2}$ as the $T_{CT}$ of input based on the size of the $T_{FT}$ received in FTRM (the selection strategy will be detailed in Section II-B and will not be elaborated here). $T_{CT}$ and $T_{FT}$ are combined in TAM as the time tag TT of the event. The TDC inside ASIC, $CCM_1$, and $CCM_2$ use the same clock signal, which is generated by a 50 MHz clock signal from a crystal OSC entering the phase locked loop (PLL) in FPGA. Among them, $CCM_1$ and $CCM_2$ count according to the rising edge and falling edge of the clock, respectively. Another clock signal generated by the PLL serves as the synchronous clock for STEM, FTRM, CTSM, TAM, RTTCM, and TTFM. A third clock signal generated by the PLL serves as the synchronous clock for TTFM, HM, SFM, and SAM.

With the method mentioned above, the TT of the four-channel input from ASIC can be obtained. After obtaining the TT of four channels in RTTCM, specify one of the channels as the reference input channel and the remaining three channels as the event input channel. RTTCM subtracts the time tags of the reference channel from the time tags of the event input channel to obtain the relative time tags of the event channel. There are three TTFMs that store the relative time tags of three event input channels generated by RTTCM. The relative time tags of three channels are entered into HM for histogram statistics. The histogram statistics results are stored in SFM and then sent to the upper computer through SAM.

### B. Timing Constraints Combing Coarse and Fine Time

FPGA, based on the $T_{FT}$ and $F_{CC}$ received from ASIC, needs to satisfy a certain timing relationship to accurately obtain the $T_{CT}$ of the Input. A detailed explanation is provided in Fig. 2(b). $CCM_1$ and $CCM_2$ count based on the rising and falling edges of the $C_{co}$, respectively. The $C_{re}$ of ASIC has the same clock cycle as $C_{co}$, denoted as $T_P$. Although $C_{re}$ and $C_{co}$ come from the same output of the PLL, there is a certain phase lag when transmitted from FPGA to ASIC TDC, denoted as $T_{D1}$. After the event $Hit_A$ enters ASIC from the Input, the $T_{FT}$ is obtained on ASIC. $T_{FT}$ is the time interval between the rising edge of the Input relative to the nearest $C_{re}$. The obtained $T_{FT}$ is sent to FPGA's FTRM through STEM. After the event $Hit_A$ enters ASIC from Input, after a certain conversion time $T_{cov}$, ASIC sends the $F_{CC}$ to the registers $Reg_1$ and $Reg_2$ inside FPGA. $Reg_1$ and $Reg_2$ use this signal as the clock signal to read $CCM_1$ and $CCM_2$. The time elapsed is denoted as $T_{D2}$, and then the value of $CCM_1$ or $CCM_2$ is selected based on $T_{FT}$ as the coarse time $T_{CT}$ for event $Hit_A$. As shown in Fig. 2(b), when the formula is satisfied

$$T_{D1} + T_{FT} + T_{cov} + T_{D2} < T_P. \tag{1}$$

The correct $T_{CTA}$ can be obtained from $CCM_1$, as $CCM_1$ only counts at the rising edge of $C_{co}$, where $CCM_1$ is stable. Due to $Hit_A$ appearing in the first half of the ASIC reference clock cycle, and the ASIC reference clock cycle being the same as the FPGA coarse counter clock cycle, there are

$$T_{FT} \le T_P \,/\, 2. \tag{2}$$

Based on (1) and (2)

$$T_{D1} + T_{cov} + T_{D2} < T_P \,/\, 2. \tag{3}$$

Similarly, when an event occurs in the second half cycle of the ASIC reference clock, such as $Hit_B$, as shown in Fig. 2(b), when the formula is satisfied

$$T_{D1} + T_{FT} + T_{cov} + T_{D2} < (1 + 1 \,/\, 2) \times T_P. \tag{4}$$

It is possible to obtain the correct $T_{CTB}$ from $CCM_2$, as $CCM_2$ only counts at the falling edge of $C_{co}$, at which point $CCM_2$ is stable. Due to $Hit_B$ appearing in the latter half of

the ASIC reference clock cycle, and the ASIC reference clock cycle being the same as the FPGA counter clock cycle, there are

$$T_{\mathrm{P}} \,/\, 2 \le T_{\mathrm{FT}} \le T_{\mathrm{P}}. \tag{5}$$

Based on (4) and (5)

$$T_{\mathrm{D1}} + T_{\mathrm{cov}} + T_{\mathrm{D2}} < T_{\mathrm{P}} \,/\, 2. \tag{6}$$

In summary, when the period $T_P$ of $C_{\mathrm{co}}$ satisfies (6), the $T_{\mathrm{CT}}$ of the event can be correctly obtained from either $\mathrm{CCM}_1$ or $\mathrm{CCM}_2$ of FPGA, thereby correctly obtaining the TT of the event.

### C. Relative Time Tag Acquisition

To obtain relative time tags, it is necessary to specify any one of the signals in ASIC as the reference signal. After determining the reference signal, for the remaining three channels, to calculate the relative time tags of events in each channel, it is only necessary to subtract the time tag of the reference signal from the time tag of the event occurring in that channel. The time required from the event entering ASIC to FPGA correctly obtaining the time tag of the event can vary by nanoseconds, which can lead to a phenomenon where the event signal appears later in time than the reference signal, but it may happen that FPGA obtains the time tag of the event signal from ASIC ahead of time, but has not yet obtained the time tag of the reference signal. If the RTTCM is performed immediately at this time, due to the current reference time tag not being updated to the latest time tag, it will lead to an error in calculating the relative time tag of the event.

To avoid errors in calculating the relative time tags of events, an RTTCM is used, as shown in Fig. 3(a). After entering RTTCM, TT enters multiple serial registers Reg[$n$:0], each of which delays the TT by one Clk cycle before passing it to the next stage of Reg. The signal $\mathrm{TT_D}$ after multiple Reg delays enters $\mathrm{CP_1}$, $\mathrm{CP_2}$ and $\mathrm{AD_1}$–$\mathrm{AD_3}$. The TT generated for the specified reference signal is denoted as $\mathrm{TT_R}$. After entering the RTTCM, it passes through two cascaded registers, $\mathrm{Reg_A}[n{:}0]$ and $\mathrm{Reg_B}[n{:}0]$. The synchronous clock of $\mathrm{Reg_A}[n{:}0]$ and $\mathrm{Reg_B}[n{:}0]$ is the signal after the AD of Clk and $F_{\mathrm{TTR}}$, where $F_{\mathrm{TTR}}$ is a pulse signal generated when FPGA receives a $\mathrm{TT_R}$. Through $\mathrm{Reg_A}[n{:}0]$, $\mathrm{Reg_B}[n{:}0]$, and AD, it is possible to achieve the output $\mathrm{TT_{RD1}}$ of $\mathrm{Reg_A}[n{:}0]$ as the last $\mathrm{TT_R}$ that appeared. The output $\mathrm{TT_{RD2}}$ of $\mathrm{Reg_B}[n{:}0]$ is the third-to-last $\mathrm{TT_R}$. Compare the size of $\mathrm{TT_D}$ and $\mathrm{TT_R}$ in $\mathrm{CP_1}$. If $\mathrm{TT_D}$ is larger than $\mathrm{TT_R}$, $\mathrm{CP_1}$ outputs 1 to drive $\mathrm{SM_2}$ to switch to the $A$ input; otherwise, it maintains the $B$ input. Compare the size of $\mathrm{TT_D}$ and $\mathrm{TT_{RD1}}$ in $\mathrm{CP_2}$. If $\mathrm{TT_D}$ is greater than $\mathrm{TT_{RD1}}$, $\mathrm{CP_2}$ outputs 1 to drive $\mathrm{SM_1}$ to switch to the $A$ input; otherwise, it remains on the $B$ input. The function of $\mathrm{AD_1}$–$\mathrm{AD_3}$ is to subtract the value of $A$ from the value of $B$ as an output. Through the above method, the relative time tag of any event can be correctly obtained.

The relative time tag of each signal channel can be correctly calculated through the schematic shown in Fig. 3(a), and the timing relationship it should satisfy is shown in Fig. 3(b). When the reference signal (channel 4 of ASIC specified in this article is designated as the reference signal input channel) appears with pulses $A, C, D, E$, and the event input channel 1 appears with pulse $B$, FPGA obtains TT of the reference signal and event signal through $T_{\mathrm{To}}$ as $A_0, A_1, A_2, A_3$, and $B_0$, respectively,

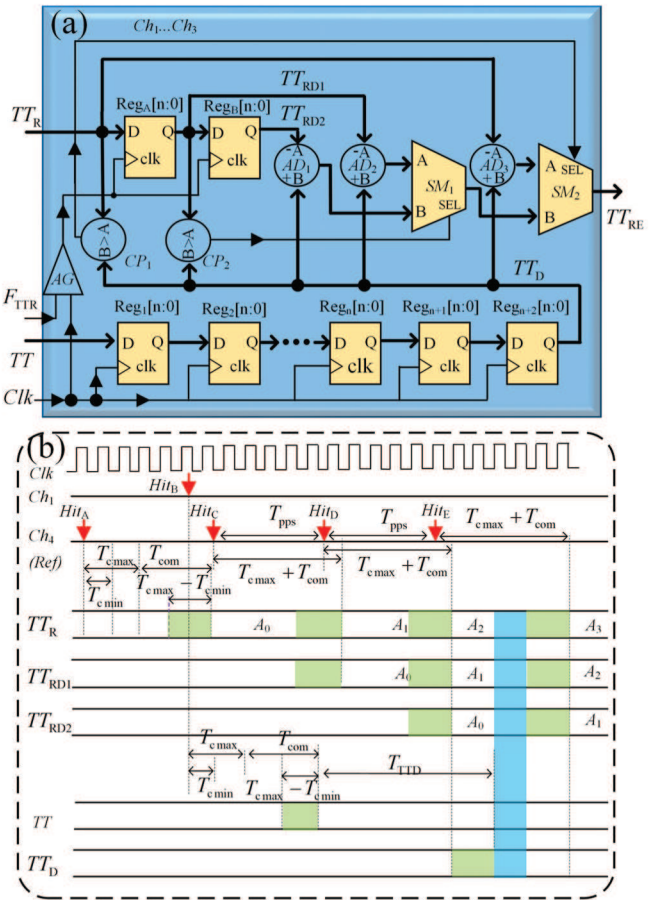


Fig. 3. Relative time tag calculation. (a) Schematic of relative time tag operation. (b) Timing diagram of relative time tag operation.

$$T_{\mathrm{To}} = T_{\mathrm{cov}} + T_{\mathrm{com}} \tag{7}$$

where $T_{\mathrm{cov}}$ is the conversion time required for ASIC to generate the fine time tag for the pulse signal, and $T_{\mathrm{com}}$ is the communication time required for ASIC to transfer the fine time tag to FPGA after generating the fine time tag for the pulse signal. According to the data sheet of ASIC [32], $T_{\mathrm{cov}}$ is an interval, so $T_{\mathrm{To}}$ is also an interval. The update time of the event signal and the reference signal time tag is also within a certain interval, as shown in the green shaded area in Fig. 3(b). The signal can be updated at any time within the shaded area. When the event time tags after the delay falls within the blue interval shown in the diagram, the relative time tags of the event can be calculated correctly. Because at this time, the reference time tags of $\mathrm{Hit_A}$, $\mathrm{Hit_C}$, and $\mathrm{Hit_D}$ have all reached their corresponding positions and remain in a stable state, the time tag corresponding to $\mathrm{Hit_B}$ only needs to be compared for comparison purposes. In order to obtain the correct relative

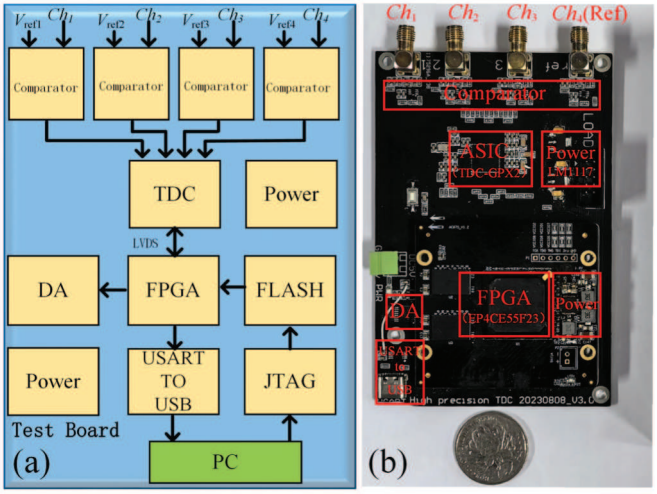


Fig. 4. Experimental prototype. (a) Schematic of PCB. (b) PCB.

time tags, the following relationship needs to be satisfied:

$$\begin{cases} T_{\text{cmax}} + T_{\text{com}} + T_{\text{TTD}} - (T_{\text{cmax}} - T_{\text{cmin}}) \geq T_{\text{cmax}} + T_{\text{com}} + T_{\text{pps}} \\ T_{\text{cmax}} + T_{\text{com}} + T_{\text{TTD}} \leq T_{\text{cmin}} + T_{\text{com}} + 2T_{\text{pps}} \end{cases} \tag{8}$$

where $T_{\text{pps}}$ is the minimum width between two consecutive pulses that ASIC can correctly process. Equation (8) is simplified to

$$\begin{cases} T_{\text{TTD}} \geq T_{c\,\text{max}} - T_{c\,\text{min}} + T_{\text{pps}} \\ T_{\text{TTD}} \leq 2T_{\text{pps}} - (T_{c\,\text{max}} - T_{c\,\text{min}}). \end{cases} \tag{9}$$

Therefore, based on (9), the allowable delay range for the variable can be obtained. By considering the clock period of Clk shown in Fig. 3(a), you can select the appropriate number of registers. For example, if the allowable delay range is 15–30 ns and the Clk period is 10 ns, you can choose to use either two or three registers to delay the TT, thereby correctly obtaining the relative time tag of the event.

### D. Histogram Statistics

Histogram statistics are also implemented as a crucial feature in the proposed digital acquisition system (DAS), performing real-time histogram statistics within FPGA for data preprocessing can effectively compress the data volume and facilitating data transmission and storage. The principle of event distribution histogram statistics uses an FPGA state machine design method. Related work can be found in our group's previous publications [14].

## III. Experimental Results

An experimental prototype was designed and built in order to validate the proposed DAS. The prototype, as shown in Fig. 4, features an FPGA development board with an Altera Cyclone 4 series chip (EP4CE75F23I7N) and an AMS TDC-GPX2 ASIC chip. It should be noted that the main task of an FPGA is to communicate with an ASIC, perform histogram statistics, and perform simple coarse counting. Most mainstream FPGA models from manufacturers, such as Altera and Xilinx, can meet these requirements. As for the selection of ASIC, currently commercially available ones with good performance indicators include TDC-GPX, TDC-GPX2, and MS1052NA, all of which can be used in this study.

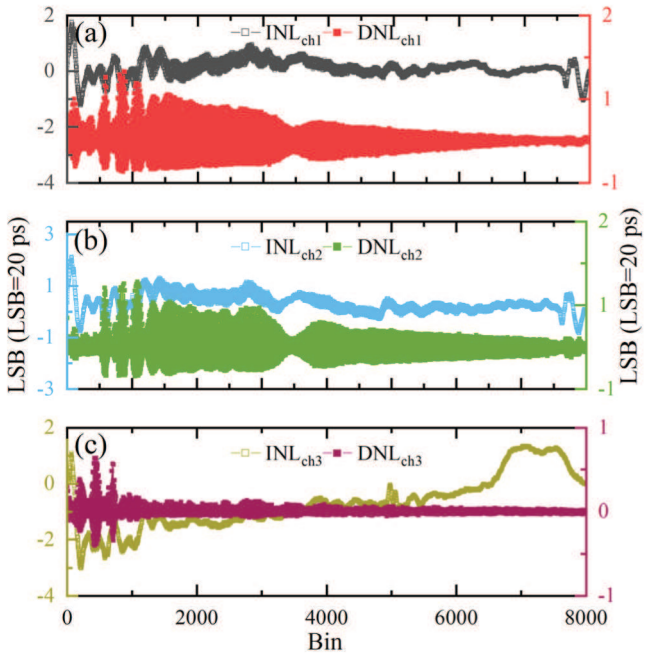


Fig. 5. Nonlinear test results. INL and DNL of (a) $Ch_1$, (b) $Ch_2$, and (c) $Ch_3$.

The circuit board is equipped with four SMA input interfaces: $Ch_1$–$Ch_3$ for event signal inputs and $Ch_4$ for the reference signal input. It has a 5 V power supply interface and communicates with the host computer via a serial port using a CH340E chip. For parameter testing, a Tektronix AFG31000 series arbitrary waveform generator was used to generate the reference signal and delay-adjustable event input signals. A single-photon detector serves as the random pulse signal generator. In addition, a self-made temperature-controlled box is used for temperature regulation of the acquisition system.

In this work, the maximum counting rate is 50 MHz, and the power consumption is 60–450 mW. The histogram statistics are completed internally in FPGA. Due to the limitation of the FPGA's internal RAM resources, the histogram statistics bin length for each channel is 8000. In the least significant bit (LSB) = 20 ps working mode, the maximum allowable time delay is 160 ns. Therefore, the test delays are 0–150 ns with a step size of 10 ns. The allowable working temperature range of ASIC involved in this work is 0 °C–80 °C. When ASIC enters stable operation, even if the ambient temperature drops to around 0°, the internal temperature of ASIC is around 25 °C due to heat generation during operation. Considering the safety of the device, the temperature range for testing work is 25 °C–65 °C.

### A. Nonlinearity

As shown in Fig. 5, the nonlinearity test of the acquisition system was conducted using the code density method. The

code density method is based on large sample statistical properties, allowing for the averaging of nonideal factors of the system through a large number of random input events, thereby providing a comprehensive evaluation of the acquisition system's performance. In this study, a single-photon avalanche diode (SPAD) was used to generate random event signals, which were split into three and fed into the three event input channels of the acquisition system. The AFG31000A was used to produce a 5 MHz signal as the reference signal. With the acquisition system resolution set to 20 ps, the 5 MHz reference signal can cover 8000 bins of the acquisition system designed in this study. A histogram of time tag distribution was collected over 100 s. It should be noted that in nonlinearity testing using the code density method, higher photon counts bring conditions closer to the ideal scenario, thereby improving result accuracy. In each test, the actual recorded total number of photons is 120 million. Using the time distribution histogram, the nonlinearity of 8000 bins in each channel of the acquisition system was determined. This is done according to the formula

$$\begin{cases} \mathrm{DNL}(i) = (n_i - n_s)/n_s \\ \mathrm{INL}(i) = \sum_{j=0}^{i} \mathrm{DNL}(j) \end{cases} \tag{10}$$

where $n_s$ represents the average number of photons per bin across the 8000 bins and $n_i$ represents the actual number of photons in the $i$th bin. The integral nonlinearity (INL) and differential nonlinearity (DNL) for each channel were obtained. From Fig. 5, it can be seen that the peak-to-peak values of the INL for the three channels are 3.0, 3.0, and 4.3 LSB, respectively, while the peak-to-peak values of the DNL are 1.2, 1.3, and 1.0 LSB. These results indicate good linearity performance across all three channels.

### B. Precision

Using a signal generator to produce two signals, one is fed into $Ch_4$ as the reference signal, while the other signal is split into three and fed into $Ch_1$–$Ch_3$ of the acquisition system as event signals. Both signals have a frequency set to 5 MHz, with the event signals delayed relative to the reference signal from 0 to 150 ns, with a step size of 10 ns. For each delay case, continuous measurements are taken for 2 s. The precision or root mean square resolution can be assessed using the standard deviation ($\delta$)

$$\delta^2 = \frac{1}{N-1} \sum_{1}^{N} (x_k - X_{\mathrm{mean}})^2 \tag{11}$$

where $N$ is the total number of measurements, $x_k$ is the time result of the $k$th measurement, and $X_{\mathrm{mean}}$is the average of the measurement results.

The results are shown in Fig. 6. During the process of the event signals delayed relative to the reference signal from 0 to 150 ns, with a step size of 10 ns, the measurement results fluctuate around the real measurement results. The maximum standard deviations of the measurement results for three channels are 28, 24, and 24 ps, respectively.

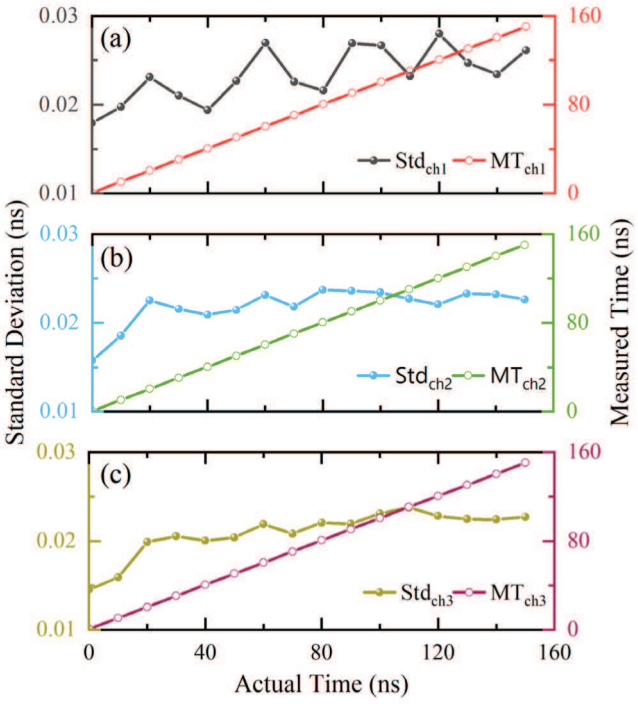


Fig. 6. Actual time, measured time, and standard deviation of the measurement. (a) $Ch_1$. (b) $Ch_2$. (c) $Ch_3$. $MT_{ch1}$: measured time of channel 1 and $Std_{ch1}$: standard deviation of channel 1.

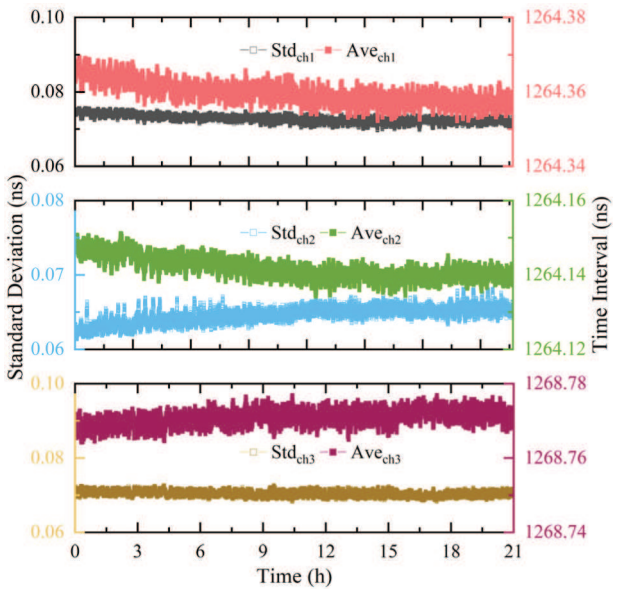


Fig. 7. Results of long-term stability testing. (a) $Ch_1$. (b) $Ch_2$. (c) $Ch_3$.

### C. Long-Term Stability

One channel of the signal generator was used as the reference signal for the acquisition system, while another channel was split into three and fed into the three event input channels of the acquisition system. The time intervals between the event signals and the reference signal were kept constant. The actual time interval measured in this experiment is around 1260 ns. A set of measurement results was generated at a frequency of 0.5 Hz over a continuous period of more than 21 h. The higher

TABLE I
COMPARISON WITH REPORTED HIGH-PRECISION TDCS

| Ref-year | Platform | LSB (ps) | Range（ns） | INL (LSB) | DNL (LSB) | Precision（ps） | FoM |
|---|---|---|---|---|---|---|---|
| [31]-2017 | Kintex-7 | 280 | $37\times10^3$ | NA | [-0.4,0.4] | 80-100 | NA |
| [32]-2020 | Virtex-5 | 46.9 | 6 | [-7.2,4.3] | [-0.78,0.76] | 35.5 | $5.4\times10^{-11}$ |
| [33]-2021 | Artix-7 | 22.2 | $262\times10^3$ | [-2.75,1.24] | [-0.95,1.19] | 26.04 | $1.2\times10^{-6}$ |
| [34]-2022 | Artix-7 | 10 | $164\times10^3$ | [-0.13,0.15] | [-2.26,3.54] | 17 | $9.9\times10^{-4}$ |
| [35]-2022 | Cyclone 10 | 5.7 | 100 | [-9.98,11.14] | [-0.96,2.9] | 4.8 | $2.3\times10^{-6}$ |
| [36]-2023 | Kintex-7 | 6.5 | 50 | [-1,4] | [-15,15] | 6.4 | $1.4\times10^{-7}$ |
| [37]-2010 | ASIC-65nm | 4.8 | 0.615 | [-1,3.3] | [-1,1] | NA | NA |
| [38]-2013 | ASIC-65nm | 3.75 | 480 | [-2.3,2.3] | [-0.9,0.9] | NA | NA |
| [39]-2014 | ASIC-130nm | 6.98 | 14 | [-1.5,1.5] | [-0.8,0.8] | 20.8 | $1.6\times10^{-6}$ |
| [40]-2016 | ASIC-65nm | 6 | 98 | [-0.1,0.5] | [-0.1,0.12] | 11 | $6.3\times10^{-2}$ |
| [41]-2019 | ASIC-180nm | 48.8 | 330 | [-1.67,0.89] | [-0.48,0.48] | 62.37 | $3.4\times10^{-9}$ |
| [42]-2019 | ASIC-40nm | 33-120 | 491 | [-1.8,3.8] | [-0.45,0.45] | 208 | $8.5\times10^{-11}$ |
| [43]-2020 | ASIC-180nm | 50 | $13.1\times10^3$ | [-0.6,0.71] | [-0.47,0.47] | 36.5 | $3.9\times10^{-7}$ |
| **This Work** | **Cyclone4+ASIC** | **20** | **$430\times10^9$** | **[-3,1.3]** | **[-0.6,0.7]** | **30** | $3.1\times10^{-3}$ |

the frequency of use, the longer the testing time, and the better the test results can reflect the real situation. The selection of this testing parameter was determined based on consideration of practical requirements and operational constraints. The results are shown in Fig. 7. The maximum standard deviations for three channels were 76, 68, and 72 ps, respectively. The peak-to-peak values of the measurement results were 17, 17, and 13 ps. These results demonstrate the acquisition card's good long-term stability.

### D. Temperature Stability

One channel of the signal generator was used as the reference signal for the acquisition system, while another channel was split into three and fed into the three event input channels of the acquisition system. The time intervals between the event signals and the reference signal were kept constant. The acquisition system was placed in a self-made temperature-controlled box, and the temperature of the ASIC chip was changed from 25 °C to 65 °C in 1 °C increments. At each temperature, measurements were continuously taken for 2 s, and the average and standard deviation of all data within the 2-s interval were calculated as the data for that temperature. The results are shown in Fig. 8. The maximum standard deviations for three channels were 30, 31, and 31 ps, respectively. The peak-to-peak values of the measurement results were 7, 13, and 12 ps. These results demonstrate the acquisition card's good temperature stability.

As shown in Table I, there are many TDC implementation architectures in the literature, each of which aims to optimize the given indicator parameters, making it difficult to make a relatively objective and comprehensive comparison of these architectures. Therefore, Table I has added the figure of merit (FoM), which can be compared more

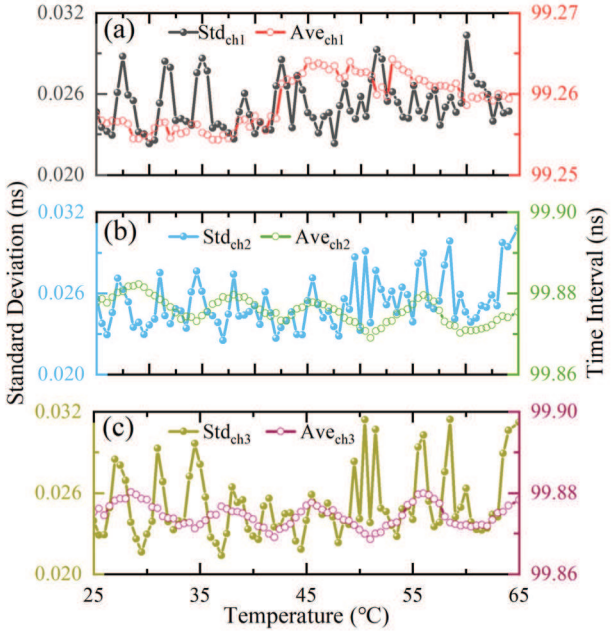


Fig. 8. Temperature stability test. (a) $Ch_1$. (b) $Ch_2$. (c) $Ch_3$.

objectively with other works. The definition of FoM is as follows:

$$\text{FoM} = \frac{(\text{Measurement Range})^{0.5}}{\text{LSB}^3 \times \text{Precision}^3 \times \text{INL}^2 \times \text{DNL}^2}. \quad (12)$$

The unit of Measurement Range is picoseconds, Precision is measurement accuracy, LSB is resolution, INL is integral nonlinearity, and DNL is differential nonlinearity. From the FoM indicators in Table I, it can be seen that work [40] has better indicators than ours. They are based on ASIC and have achieved LSB of 6 ps, accuracy of 11 ps, Measurement Range of 98 ns, INL of [−0.1, 0.5]LSB, and DNL of [−0.1, 0.12]LSB.

Our work ranks second in terms of indicators in comparison and has certain advantages. It has outstanding advantages in measurement range while ensuring resolution, accuracy, and nonlinearity.

## IV. Conclusion

Compared with previous TDC research, as shown in Table I, which primarily relies on FPGA or ASIC, this article proposes a new TDC implementation architecture that combines FPGA-based coarse counting with ASIC-based fine counting. The TDC implemented with this architecture not only retains the advantages of traditional ASIC-based TDCs, such as high measurement accuracy, uniform bin width, and good stability, but also significantly extends the measurement range of the TDC. The coarse counting is implemented within FPGA, reducing the time required to transfer time tags from ASIC to FPGA, improving communication efficiency, and enhancing the counting rate of ASIC. In addition, a DAS was designed based on this TDC architecture, with corresponding methods for relative time tag calculation and histogram statistics proposed. Finally, a prototype with three event input channels and one reference signal input channel was designed and fabricated. The prototype was tested for resolution, nonlinearity, long-term stability, and temperature stability.

The proposed TDC architecture offers a viable alternative for high-precision TDC design, especially in applications demanding high accuracy and a long measurement range, such as single-photon lidar systems [13]. When measuring the nonlinearity of the acquisition system, the peak-to-peak value of INL reached 4.3 LSB. Although within an acceptable range, noticeable fluctuations occur, particularly at the beginning of the bin axis, as shown in Fig. 5. This may be due to interference between the event signal and the reference trigger signal, which could affect the nonlinearity measurement. The specific reasons for this need further investigation in future work. For convenience, the definitions and units of the symbols used in this article are listed in Nomenclature.

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